AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

Listing of Claims:

1. (Canceled).

2. (Currently Amended) A method for fabricating a semiconductor device comprising the steps of:

forming a conductor pattern over a semiconductor substrate;

forming a first insulation film covering the conductor pattern and having a substantially flat surface;

forming over the first insulation film a second insulation film having etching characteristics different from those of the first insulation film;

forming over the second insulation film a third insulation film having etching characteristics different from those of the second insulation film;

forming over the third insulation film a mask layer; [[and]]

forming a hole in the third insulation film, the second insulation film and the first insulation film, the step of forming the hole including a first step of etching the third insulation film, a second step of etching the second insulation film and a third step of etching the first insulation film, an etching condition at the first step being different from that at the second step;

forming a conductive material in the hole to form a conductive plug of the conductive material;

forming over the third insulation film an interconnection pattern connected to the conductive plug; and

forming a fifth insulation film over the interconnection pattern, and further comprising:

before the step of forming the first insulation film, the step of forming over the conductor pattern a fourth insulation film having etching characteristics different from those of the first insulation film, and wherein

in the step of forming the first insulation film, the first insulation film is formed over the fourth insulation film so as to cover the conductor pattern, and

in the third step of etching the first insulation film, the first insulation film is etched with the fourth insulation film as a stopper.

3. (Currently Amended) A method for fabricating the semiconductor device according to claim 2, wherein

in the step of forming the conductor patter, the conductor pattern is formed over a first region of the semiconductor substrate;

in the step of forming the fourth insulation film, the fourth insulation film is selectively formed over a side wall of the conductor pattern; and

in the third step of etching the first insulation film, the first insulation film is etched to form the opening exposing in a part of a bottom thereof a second region of the semiconductor substrate, which is other than the first region, and exposing in another part of the bottom thereof the fourth insulation film.

4. – 18. (Canceled).

19. (Previously Presented) A method for fabricating the semiconductor device according to claim 2, wherein

in the first step of etching the third insulation film, the third insulation film is etched with the second insulation film as a stopper.

20-22 (Canceled).

23. (Previously Presented) A method for fabricating a semiconductor device according to claim 2, further comprising steps of forming capacitors, bit lines and wiring layers to constitute a memory device.

24. (Previously Presented) A method for fabricating a semiconductor device according to claim 2, wherein the first insulation film comprises silicon oxide.

25. (Previously Presented) A method for fabricating a semiconductor device according to claim 2, wherein the second insulation film comprises silicon nitride.

26. (Previously Presented) A method for fabricating a semiconductor device according to claim 2, wherein the third insulation film comprises silicon oxide.

27. (Previously Presented) A method for fabricating a semiconductor device according to claim 2, further comprising steps of forming capacitors, bit lines and wiring layers to constitute a memory device.

28. (Currently Amended) A method for fabricating a semiconductor device according to claim 2, wherein

in the step of forming the hole, an etching rate of the second insulation film when the second insulation film is etched with an etching condition at the first step of etching the third insulation film is lower than an etching rate of the third insulation film at the first step of etching the third insulation film and an etching rate of the second insulation film at the second step of etching the second insulation film.